An All-Ceramic Interconnect for Use in Solid-Oxide Fuel Cell Stacks

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Abstract

This article summarizes a unique approach in which all-ceramic interconnects are used in place of metal interconnects in solid-oxide fuel cell (SOFC) stacks. The approach combines advanced SOFC materials with the manufacturing technology and infrastructure established for multilayer ceramic (MLC) packaging for the microelectronics industry. The MLC interconnect is fabricated using multiple layers of yttria-stabilized zirconia (YSZ) tape, with each layer containing conductive vias to provide for electrical current flow through the interconnect. The all-ceramic interconnect design facilitates uniform distribution of air and fuel gas to the respective electrodes of adjacent cells. The multilayer interconnects are fabricated using traditional MLC manufacturing processes. A detailed description of the processes for fabricating the all-ceramic interconnect is presented. To aid in moving from prototype fabrication to commercialization of these fuel cell systems, a detailed cost model has been used as a roadmap for commercial stack development. Cost model projections are presented for three different interconnect footprint sizes. These projections show an SOFC stack cost of less than $150 per kilowatt for the optimized SOFC stack design produced at high volume.

Keywords: *ceramics, layered structure, solid-oxide fuel cells, zirconia, interconnects.*

Introduction

Fuel cells are electrochemical devices that directly convert chemical energy into electricity. Because fuel cells operate at low voltages (less than one volt per cell), cells are stacked in series to produce usable power. In a fuel cell stack, adjacent cells are separated by interconnects. The interconnects in a stack serve three important purposes. First, they distribute the air and fuel gas to the respective electrodes. Second, they must be hermetic so that the air and fuel are not permitted to physically mix in the stack. Third, they provide an electrical path for electrons from one cell to be transported to the adjacent cell in a stack. Solid-oxide fuel cell (SOFC) stacks employ one of three approaches for the interconnects: metal interconnects, electrically conductive ceramic perovskites, or nonconducting ceramic structures containing vias for electrical conduction. Vias are electrical conduits in a planar structure that are processed by punching or drilling holes, then filling them with an electrically conductive paste. This material is then cosintered with the main body of the laminated structure.

Of the three interconnect types, clearly metal interconnects are the most widely used. However, the metal interconnects are not without technical issues, which are currently being addressed by fuel cell developers and groups performing materials research. New materials have shown a good coefficient of thermal expansion (CTE) match with the cell and reduced electrical resistance of oxide scales, but the long-term electrical conductivity of the oxide scales must be verified. In addition, the evolution of chromium-containing species from the ferritic stainless steels and subsequent deleterious reactions with the SOFC cathode remain a concern. Other areas being studied include scale adherence and corrosion resistance under oxidizing and reducing environments in the fuel cell reactant streams.[1,2] A seal material is typically used around the perimeter of the cells to eliminate the possibility of gas leakage into or out of the region adjacent to the cell electrodes. To maintain this seal, it is desirable that the CTE of the interconnect closely match that of the cell. These issues are currently being studied, with the goal of developing materials and/or operating conditions that permit the use of metal interconnects in SOFC stacks.

SOFCo-EFS (Alliance, Ohio) is developing a novel, multilayer, planar SOFC stack design that combines advanced SOFC materials with the manufacturing technology and infrastructure established for multilayer ceramic (MLC) packaging for the microelectronics industry. The basic design for the patented all-ceramic interconnect is illustrated in Figure 1. The interconnect consists of multiple dense layers of yttria-stabilized zirconia (YSZ) and provides the essential functions of electrical conduction, distribution of air and fuel flow, and gas separation. Electrical conduction is accomplished through the use of conductive vias that are fabricated into each YSZ layer; the use of conductive vias is well established in the microelectronics packaging industry. The via diameter, spacing, and number are determined by the conductivity of the via material and the amount of current flowing in an operating stack. Cosintering of the vias and zirconia layers during the fabrication of the interconnect presents complex materials issues in terms of avoiding adverse reactions and achieving shrinkage matching. In addition, the CTE must also be equal for these different materials for long-term stack reliability.

The flow of air and fuel through the interconnect is accomplished by the use of channels formed in selected layers. The

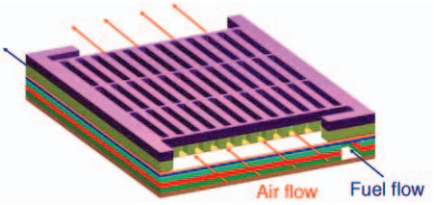

Figure 1. Schematic illustration of a multilayer co-flow interconnect.

channel width and depth (i.e., layer thickness) are determined by the reactant flow rates and the allowable pressure drop through the stack. The vias and air flow channels for a typical co-flow interconnect are shown in Figure 2. Integral gas distribution channels and other features are included in the design to facilitate the uniform distribution of reactants across the electrodes, which is essential to achieving high fuel utilization and controlling temperature gradients. Close CTE match between the interconnects and zirconia-based cells provides for effective stack sealing and improved mechanical integrity during thermal transients.

Assembly of a stack using the multilayer interconnects requires a number of steps to achieve the required seals and electrical contacts. First, a seal must be applied to keep air and fuel fed to the stack from escaping to the surrounding region, thus maintaining the effectiveness of the fuel cells. SOFCo currently uses a ceramic paste to form the seal between cells and interconnects. Figure 3 shows a ceramic interconnect with a bead of paste applied around the outside perimeter. A conductive ink is also applied to the vias to form the electrical connection to the electrodes in the adjacent cells.

In addition to the internal stack sealing, fuel cell stacks must have good seals between the manifolds and the stacks to avoid losing fuel and air to the area around the stacks. For a co-flow stack design with a single enclosure housing the air and fuel inlets, a seal must exist that does not permit air and fuel to mix in the inlet manifold. Figure 4 shows a SOFCo short stack and matching manifold. The manifold has inlet plenums (enclosures within the stacks that contain gas at a higher pressure than the region into which it will flow) to provide a constant-pressure supply of air and fuel to all cells. Sealing between the stack and manifold is accomplished with a ceramic-fiber gasket.

Interconnect Fabrication Processes

The multilayer interconnects are fabricated using established MLC manufacturing processes, including tape casting, punching, screen printing, lamination, excising, and firing. A process flow diagram depicting the basic steps that are used in fabricating the all-ceramic interconnects is shown in Figure 5. The interconnect design is well within the standard design-for-manufacturing guidelines practiced in the microelectronics packaging industry. Furthermore, the equipment needed for manufacturing interconnects of up to 20 cm is readily available.

Slip and Tape Cast Processing (Plastic–Ceramic Composites)

The initial step in the manufacture of the all-ceramic interconnect is the preparation of a slip, or slurry, that comprises high-purity zirconia powder along with poly(vinyl butyral) as the binder, butyl benzyl phthalate as the plasticizer, sodium poly(oxyethylene phenyl ether phosphate) as the dispersant, and a mixture of solvents. The slip is prepared in a two-stage process. Zirconia powder is first milled to the desired surface area and particle size distribution with some of the solvent and dispersant before being mixed with the remaining solvent, binder, and plasticizer. The zirconia slip used to make tape for the interconnect layers typically has a viscosity of 5000–7000 cP, or roughly the consistency of house paint.

Casting the tape can be accomplished in either a batch or continuous process. For large-volume production, continuous tape casters are required. The zirconia slip is poured into a reservoir behind a blade (commonly called a doctor blade) onto a moving surface. Continuous tape casters have a steel belt that loops continuously between the casting end (the end with the doctor blade) and the exit end. Often a poly(ethylene terephthalate) film is placed on the steel belt to separate it from the slip and act as the carrier. The gap between the doctor blade and the film determines the thickness of the wet tape. The wet tape continues to travel along on the moving surface through the drying section of the tape caster. Several operating variables associated with the tape caster, such as speed, temperature, and air flow, determine the final thickness and properties of the tape.[3] When the tape exits the relatively long caster (typically 12–24 m), it is dry to the touch and can then be cut to the appropriate size for subsequent operations. Zirconia tape is further conditioned in a low-temperature oven to drive off excess solvent and provide dimensional stability. At this point in the process, the tape is flexible enough for handling and does not crack with minor bending. This is a desirable characteristic of the tape that allows processing in the downstream steps without damaging it.

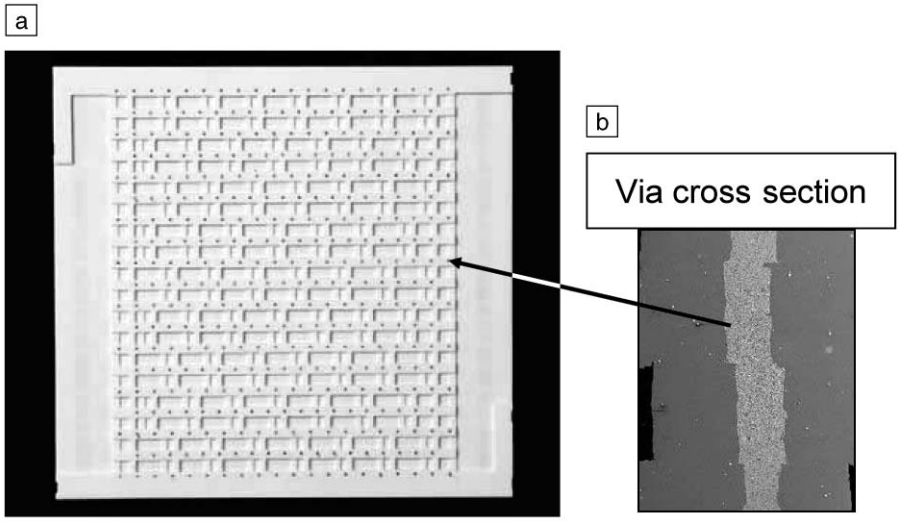

Figure 2. (a) Photograph of an interconnect (~2.4 mm thick), showing the air flow passages. (b) Cross section, through the YSZ layers, of a via (~380 μm in diameter). The image is a scanning electron micrograph in secondary electron image mode.

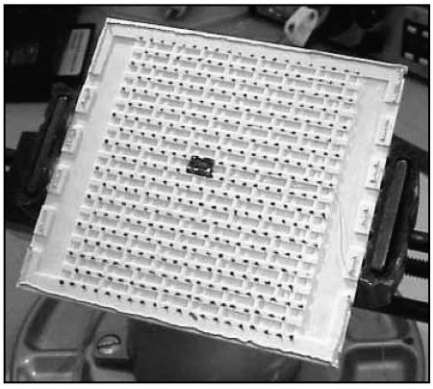

Figure 3. Air side of a parallel-flow 10-cm.-wide ceramic interconnect ready for assembly. A bead of paste is applied around the outside perimeter, and a conductive ink is applied to the vias to form the electrical connection to the electrodes in the adjacent cells.

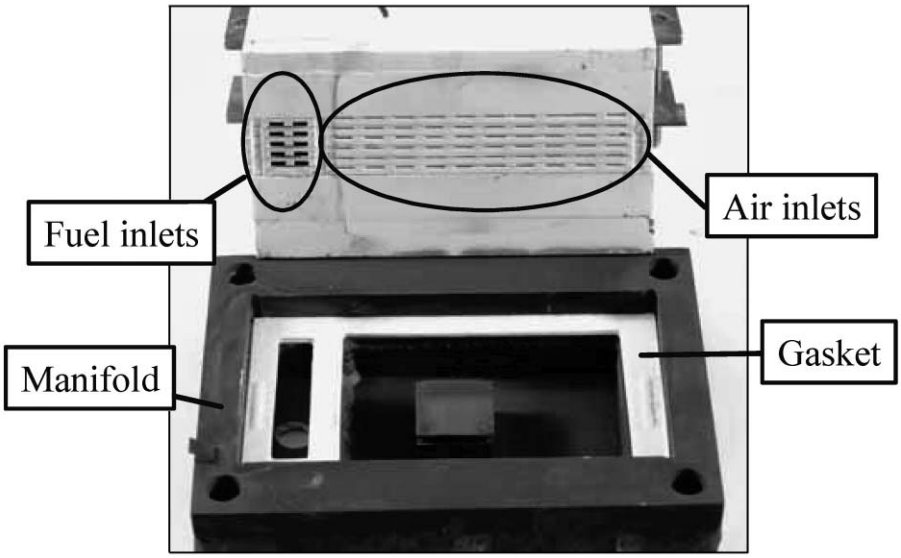

Figure 4. Manifold and stack inlet arrangement. The five-cell stack, comprised of 10 cm components, is shown with fuel and air inlets. The arrays of fuel and air inlets are created by stacking interconnects with a fuel cell between two adjacent interconnects. Including the ceramic end blocks, the stack is ~5 cm high. The matching manifold is shown lying down to permit visual access to its internal structure. The manifold internals match with the fuel and air inlets, and a gasket is used to keep air and fuel from mixing at the stack inlet face.

Tape Blanking, Printing, and Lamination

After the tape is produced, it is cut or blanked into standard sizes ready for the first round of punching. In this step, the tape blanks are punched with via and registration holes. The registration holes are used in many of the subsequent steps as a way of positioning the tape layers on the equipment to maintain proper alignment. At present, the punching operation is accomplished with a numerical punch machine for low-volume production of interconnects. These are cost-effective, especially in a prototyping situation in which minor changes may be made in the component design. For high-volume component production, the punching will likely be performed using a once-through stamping or gang punch operation on individual tape layers.

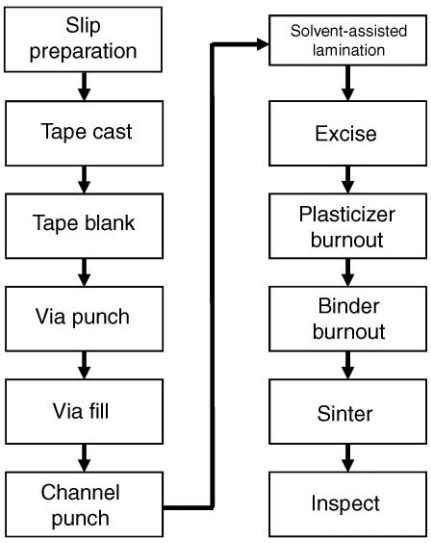

Figure 5. Interconnect fabrication process flow diagram.

Following the first punching step, the vias are filled with a conductive paste and dried in a low-temperature oven. The paste is presently made from a cermet consisting of powders of platinum and zirconia. The composition of the conductive paste was engineered to achieve the desired conductivity and to match the CTE of the YSZ interconnect. Finite element analysis was performed to determine the optimal CTE for the filled via material without introducing interfacial tensile stress to the via walls. The results suggested that the difference should be no more than 0.5×10^{-6} from the CTE of zirconia (i.e., 10.8×10^{-6}). Based on this guideline, a conductive paste was formulated with the required ratio of platinum to zirconia to achieve a CTE of approximately 10.5×10^{-6}. Figure 6 is a cross-sectional scanning electron microscopy image in backscattered mode of a via, showing the distribution of platinum particles in a zirconia matrix. The platinum is well distributed in a continuous phase throughout the via, thereby providing the required electrical path.

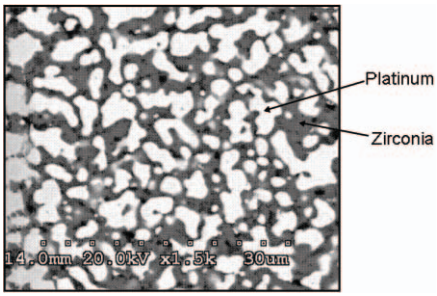

Figure 6. Cross-sectional scanning electron micrograph of a via, showing the distribution of platinum and zirconia. The platinum is well distributed in a continuous phase throughout the zirconia, thereby providing the necessary electrical path. Width of image is ~40 μm.

A second punching step follows the via filling in which the integral manifolds and flow channels are punched in the various layers. The punching pattern for each layer of the multilayer ceramic interconnect is unique. When combined into a single laminated component, the individual punched layers form the flow channels that direct the air and fuel to the respective electrode surface. The central layer acts as a separator between the air and fuel sides of the interconnect. The separator layer contains vias to conduct electric current between the air and fuel sides of the interconnect and serves as a hermetic seal between the air and fuel flow layers.

After the individual layers have undergone the second punching step, the layers are laminated together. Several different lamination options exist: the layers can be pressed together using high-pressure thermal lamination, or they can be "glued" together by means of a solvent-assisted process at room temperature using a relatively low pressure. During the early process development stage, SOFCo engineers found that excessive lamination pressure from thermal lamination caused cracks and deformation in the fired parts. When insufficient pressure was used, delaminations were found to occur. By using a lower lamination pressure in conjunction with a small amount of solvent, tape cracks, delaminations, and deformations were minimized. As a result, the current method used by SOFCo involves solvent-assisted lamination at room temperature. A small amount of solvent is used to assist in the lamination process by activating the

binder at the tape surfaces, and an intermediate pressure is applied to bring the activated surfaces together. This highlights the importance of interfacial chemistries during processing and operation.

To prepare for the next step of cofiring, the green laminates are cut or excised to size by trimming the excess material and registration holes. Three different excising techniques can be used for this application: laser cutting, diamond sawing, and hot knife excising. Laser cutting offers accurate and fast cutting along the beam path and is capable of achieving complex and intricate patterns on a variety of materials. However, laser cutting of green laminates can produce debris on the cut edge that can contaminate the interconnect. In addition, the cut edges may be slightly beveled due to the shape of the beam. Excising with a diamond saw can produce good edge quality on the green laminates. This technique has been widely used by the semiconductor industry for dicing ceramic components. A hot knife is designed specifically for cutting multilayer ceramic components in a clean-room environment. The process can produce good edge quality on the green laminates and is completely dust-free. SOFCo currently uses both hot knife excising and diamond sawing.

Cosintering Process

The next step in the MLC process is the cofiring of the green laminates. When ceramic materials are fired at elevated temperatures, they typically exhibit considerable shrinkage that must be considered in the fabrication processes. For the all-ceramic interconnect fabricated with YSZ, the shrinkage is approximately 21%. Because the via material is different from the base interconnect YSZ, its shrinkage must match that of the YSZ. In addition, the shrinkage profiles of both materials must closely match each other during sintering. This match is required at the interface between the via and the adjacent YSZ material to maintain a gas-tight structure. The via material and YSZ tape have been engineered to achieve the required shrinkage behavior. Upon defining the via composition (ratio of platinum to zirconia), the particle size distribution and surface area of the powders were varied and sintering trials were performed until the total shrinkage and shrinkage profile matched those of the interconnect YSZ material.

The interconnects are fired in a sequential batch process that includes plasticizer burnout (PBO), binder burnout (BBO), and sintering of the laminate. PBO and BBO are performed in an oven at temperatures of approximately 200°C and 400°C, respectively. Sufficient air flow is required to achieve uniform burnout of the organic constituents. The PBO and BBO steps can be combined into a single heat-treatment step by programming the oven with a suitable temperature cycle. It has been found that the PBO treatment is essential prior to sintering to relieve the residual stress of the green laminates by creating microporosity. Once the stress is relieved, the interconnects can better withstand the thermal stress generated from the temperature gradient in the sintering furnace. In addition, the use of a separate BBO step serves to eliminate the need for high air flow in the sintering furnace. Without air circulation, a uniform temperature profile can be maintained in the sintering furnace. Moreover, separation of the BBO step from the sintering operation leads to a shorter overall cycle time for the firing process, thus increasing the production output.

The cofiring operation is presently carried out by placing individual components on kiln furniture that is stacked for firing at 1350–1450°C in the batch furnace. Figure 7 shows columns of kiln furniture, containing the interconnect laminates, stacked on the floor of a high-temperature furnace prior to sintering. The use of a batch furnace works well for firing relatively small quantities of interconnects. However, for large-volume production of interconnects, a continuous furnace would be used. A typical production system might include a pusher plate tunnel kiln in which the stacked kiln furniture sits on ceramic plates moved continuously through the furnace. The pusher plates travel at a predetermined speed to maintain the desired heating profile for the parts.

After the interconnects are processed through the sintering step, a final inspection is performed. In general, an interconnect is considered acceptable for use in a fuel cell stack when it exhibits excellent flatness and low via resistance and is within dimensional tolerances. In addition, the interconnects must be free of cracks and delaminations that would otherwise degrade the performance of the stack.

Figure 7. Kiln furniture, containing fuel cell laminates, stacked on the floor of a high-temperature furnace prior to sintering. The inside dimensions of the furnace are 46 mm × 46 mm.

Manufacturing Cost Model

Using sources within the MLC industry, SOFCo has established a robust production cost model that includes the materials, labor, and equipment for each step in the high-volume manufacture of all-ceramic SOFC stacks. In addition, SOFCo has developed a number of models to evaluate stack performance (e.g., coupled thermal–electrochemical models) and integrity (e.g., finite element structural models). Using these models, SOFCo has performed extensive analyses for a number of stack design variants, many alternative low-cost materials, and different process options for key manufacturing steps. As an example, the cost model has been used to evaluate the effect of increasing the cell and interconnect sizes, from 10 cm to 15 cm to 20 cm. Figure 8 shows that the estimated cost drops significantly as the footprint increases. Examination of the cost estimates on a more detailed basis showed that the material cost per kilowatt remained about the same as the footprint increased, but the cost per kilowatt for the remaining cost elements (labor, indirect materials, and manufacturing overhead) dropped substantially. This trend was primarily due to the increased power per repeat unit (cell plus interconnect) as a result of the higher cell active area. The model has been used to evaluate other process options, such as equipment type, equipment size, and throughput. Using this model, the manufacturing cost for an optimized SOFC stack design has been projected to be less than $150 per kilowatt.

Challenges and Future Development for Low-Cost SOFC Stacks

To meet the broad commercial targets for cost and performance, several different approaches have been evaluated for reducing the cost of the manufactured components in the fuel cell stack. These approaches include scaling up manufacturing to larger cells and interconnects, introducing higher-power-density cells into stacks, and implementing lower-cost materials. While larger footprints and lower-cost materials can reduce the cost of fabricated components, increased power density has a direct impact on the number of components required for a given power

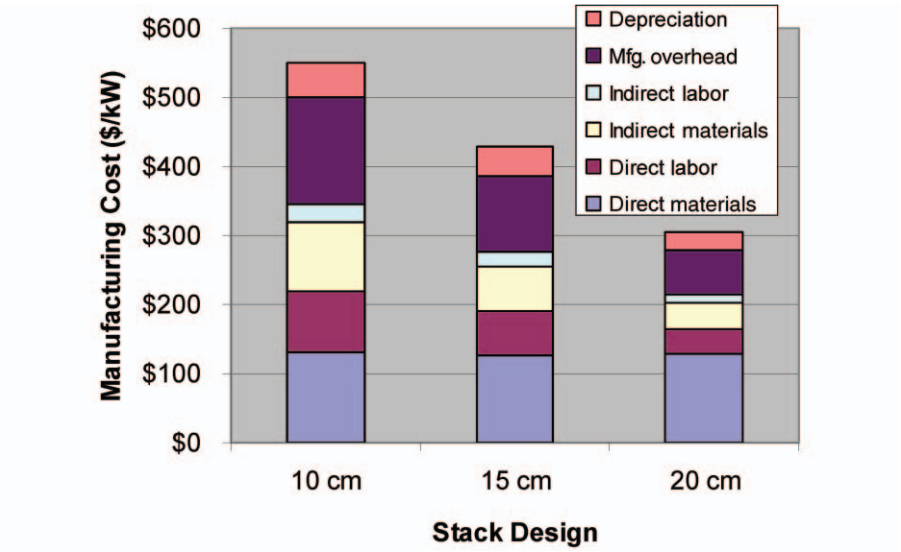

Figure 8. Cost model projections for the impact of increasing the footprint for high-volume production of all-ceramic solid-oxide fuel cell stacks.

output. For example, doubling the power density of a stack will double its power output at fixed operating conditions, which will cut the cost per kilowatt in half. Doubling the power density could be accomplished by reducing the electronic resistance of the stack by 50% through cell material improvements, better cell stacking procedures, and lower interconnect resistance. No other changes in the material selection or fabrication processes can have as significant an impact on the cost of the final product as the power density.

Larger interconnects and cells are being evaluated for use in SOFC stacks. Design factors such as structural integrity and air-side pressure drop are taken into consideration in the evaluations, as are fabrication factors such as ease of handling and conformance with standard manufacturing equipment. Currently, prototype components are being manufactured, after which they will be structurally evaluated and tested in fuel cell stacks to determine their acceptability for commercial use.

Greater than 90% of the material within the SOFCo stack is YSZ. To date, most of the interconnects fabricated for SOFCo have used an expensive powder from a single supplier. Several lower-cost sources of YSZ for the interconnect will be evaluated in the near future. To qualify a new powder, prototype parts must be made using the candidate powder, and production tests must demonstrate acceptable performance.

The final area for materials substitution for cost reduction will be the replacement of the via materials currently in use. As mentioned previously, the MLC interconnect was developed using a platinum-YSZ cermet for the conducting vias. Although expensive, this material was found to be compatible with the YSZ material in terms of sintering behavior (i.e., shrinkage match) and CTE. As a result, rapid development of the MLC interconnect was facilitated by using the Pt-YSZ via materials. Efforts are now being directed toward the development and implementation of lower-cost via materials. Prototype interconnects with the fuel- and air-side vias replaced with a nickel cermet and a perovskite oxide, respectively, have been produced and tested. The interconnect design and via compositions are being modified to optimize performance.

Conclusion

Significant progress has been made to demonstrate the potential use of ceramic interconnects for SOFC applications. SOFCo's all-ceramic design uses multilayer ceramic fabrication processes that have been used in the microelectronics packaging industry for years. Current improvements to the components include the implementation of less-expensive materials for the YSZ body of the interconnect and for the platinum-based via materials as well as the incorporation of larger components. Component fabrication is moving from low-volume prototyping to higher-volume manufacturing to support the commercialization of fuel cell power systems. SOFCo forecasts that implementing these improvements and manufacturing at high volumes will lead to an SOFC stack costing less than $150 per kilowatt, thus meeting a key commercial target.

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